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EXAMINER	
MOORE JR, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/036,622	RASHID ET AL.	
	Examiner	Art Unit	
	Michael J. Moore, Jr.	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *39-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39-68 and 71-79* is/are rejected.

7)☒ Claim(s) *69 and 70* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 1/26/06 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner has considered the information disclosure statement.

Claim Objections

Amendments made by Applicant to obviate the claim objections presented in the previous Office Action are proper and have been entered. These objections have been withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims **39-57 and 71-79** are rejected under 35 U.S.C. 102(e) as being anticipated by Mann et al. (U.S. 6,212,165) (hereinafter "Mann"). *Mann* teaches all of the limitations of the specified claims with the reasoning that follows.

Regarding claim **39**, "an apparatus" is anticipated by network device 70 (apparatus) shown in Figure 2.

"A set of input ports" is anticipated by input ports 12 shown in Figures 2 and 3.

"A FIFO storage buffer" is anticipated by the input queue 36 (FIFO storage buffer) shown in Figure 3.

"Request logic coupling the set of input ports to the FIFO storage buffer" is anticipated by controller 34 (request logic) that couples input ports 12 to input queue 36 as shown in Figure 3.

"A memory in communication with the request logic, wherein the memory concurrently maintains a plurality of pointers, wherein each pointer in the plurality of pointers corresponds to a different location in the FIFO storage buffer for storing data from an input port in the set of input ports" is anticipated by the RAM 50 (memory) of the input queue 36 (FIFO storage buffer) shown in Figure 4 that maintains a plurality of pointers WRITE_POINTER_N as spoken of on column 5, lines 31-54.

Lastly, "wherein the request logic simultaneously writes data to the FIFO storage buffer for at least two of the input ports" is anticipated by controller 34 (request logic) of Figure 3 that receives data from the input ports and writes to up to four segments of the input queue at any one time (simultaneously) as spoken of on column 5, lines 14-19, as well as column 6, lines 38-40, and column 8, lines 23-31.

Regarding claim **40**, "a first entry that maintains a pointer corresponding to a first location in the FIFO storage buffer for storing a first set of data from an input port in the set of input ports" is anticipated by WRITE_POINTER_1 shown in Figure 4 that corresponds to the first segment 52 (location) in input queue 36 where data input from the input ports is written as spoken of on column 5, lines 39-54.

Lastly, "a second entry that maintains a pointer corresponding to a second location in the FIFO storage buffer for storing a second set of data from an input port in the set of input ports" is anticipated by WRITE_POINTER_2 of Figure 4 that corresponds to the second segment 52 (location) in input queue 36 where data input from the input ports is written.

Regarding claim **41**, "a third entry that maintains a pointer corresponding to a third location in the FIFO storage buffer for storing a third set of data from an input port in the set of input ports" is anticipated by WRITE_POINTER_3 of Figure 4 that corresponds to the third segment 52 (location) in input queue 36 where data input from the input ports is written.

Lastly, "a fourth entry that maintains a pointer corresponding to a fourth location in the FIFO storage buffer for storing a fourth set of data from an input port in the set of input ports" is anticipated by WRITE_POINTER_N of Figure 4 that corresponds to the Nth segment 52 (location) in input queue 36 where data input from the input ports is written.

Regarding claim **42**, "wherein the memory maintains a data identifier for each pointer in the plurality of pointers" is anticipated by the data segments 52 of Figure 4 that each correspond to a particular pointer.

Regarding claim **43**, "wherein each data identifier identifies a data source" is anticipated by the data segments 60 shown in Figure 5 containing frame data 62 and attributes 64 corresponding to a particular input port (data source) as spoken of on column 5, lines 30-39.

Regarding claim **44**, "wherein the memory is a content addressable memory" is anticipated by the RAM 50 of Figure 4.

Regarding claim **45**, "wherein the request logic and the storage buffer are included in a multiple port memory" is anticipated by controller 34 (request logic) and input queue 36 (storage buffer) within multiple input/single output FIFO queue 10 of Figure 3.

Regarding claim **46**, "an apparatus" is anticipated by network device 70 (apparatus) shown in Figure 2.

"A set of input ports" is anticipated by input ports 12 shown in Figures 2 and 3.

"A FIFO storage buffer" is anticipated by the input queue 36 (FIFO storage buffer) shown in Figure 3.

"Request logic coupling the set of input ports to the FIFO storage buffer" is anticipated by controller 34 (request logic) that couples input ports 12 to input queue 36 as shown in Figure 3.

"Wherein the request logic simultaneously writes data to the FIFO storage buffer for at least two of the input ports" is anticipated by controller 34 (request logic) of Figure 3 that receives data from the input ports and writes to up to four segments of the input queue at any one time (simultaneously) as spoken of on column 5, lines 14-19, as well as column 6, lines 38-40, and column 8, lines 23-31.

"A memory in communication with the request logic, wherein the memory concurrently maintains a plurality of pointers, wherein each pointer in the plurality of pointers corresponds to a different location in the FIFO storage buffer for storing data

from an input port in the set of input ports" is anticipated by the RAM 50 (memory) of the input queue 36 (FIFO storage buffer) shown in Figure 4 that maintains a plurality of pointers WRITE_POINTER_N as spoken of on column 5, lines 31-54.

"Wherein the memory maintains a data identifier for each pointer in the plurality of pointers" is anticipated by the data segments 52 (identifiers) of Figure 4 that each correspond to a particular pointer.

"Wherein each data identifier identifies a data source" is anticipated by the data segments 60 shown in Figure 5 containing frame data 62 and attributes 64 corresponding to a particular input port (data source) as spoken of on column 5, lines 30-39.

"A first entry that maintains a pointer corresponding to a first location in the FIFO storage buffer for storing a first set of data from an input port in the set of input ports" is anticipated by WRITE_POINTER_1 shown in Figure 4 that corresponds to the first segment 52 (location) in input queue 36 where data input from the input ports is written as spoken of on column 5, lines 39-54.

Lastly, "a second entry that maintains a pointer corresponding to a second location in the FIFO storage buffer for storing a second set of data from an input port in the set of input ports" is anticipated by WRITE_POINTER_2 of Figure 4 that corresponds to the second segment 52 (location) in input queue 36 where data input from the input ports is written.

Regarding claim **47**, "a third entry that maintains a pointer corresponding to a third location in the FIFO storage buffer for storing a third set of data from an input port

in the set of input ports" is anticipated by WRITE_POINTER_3 of Figure 4 that corresponds to the third segment 52 (location) in input queue 36 where data input from the input ports is written.

Lastly, "a fourth entry that maintains a pointer corresponding to a fourth location in the FIFO storage buffer for storing a fourth set of data from an input port in the set of input ports" is anticipated by WRITE_POINTER_N of Figure 4 that corresponds to the Nth segment 52 (location) in input queue 36 where data input from the input ports is written.

Regarding claim **48**, "wherein the memory is a content addressable memory" is anticipated by the RAM 50 of Figure 4.

Regarding claim **49**, "wherein the request logic and the storage buffer are included in a multiple port memory" is anticipated by controller 34 (request logic) and input queue 36 (storage buffer) within multiple input/single output FIFO queue 10 of Figure 3.

Regarding claim **50**, "a sink port" is anticipated by network device 70 (sink port) shown in Figure 2.

"A multiple entry point FIFO having a plurality of data inputs in communication with a set of input ports to simultaneously accept and store data for at least two of the input ports" is anticipated by multiple input/single output FIFO queue 10 (multiple entry point FIFO) of Figure 3 that receives a plurality of data input from ports 12 via port combiner 30 and uses controller 34 to write to up to four segments of the input queue at

any one time (simultaneously) as spoken of on column 5, lines 14-19, as well as column 6, lines 38-40, and column 8, lines 23-31.

Lastly, "an output port coupled to the multiple entry point FIFO to receive the data from the multiple entry point FIFO and transmit the data on a communications link" is anticipated by input buffer 40 (output port) of Figure 3 that forwards data directed from the ports 12 to switching fabric 42 as spoken of on column 4, lines 38-43.

Regarding claim **51**, "a FIFO storage buffer" is anticipated by the input queue 36 (FIFO storage buffer) shown in Figure 3.

"Request logic coupling the set of input ports to the FIFO storage buffer" is anticipated by controller 34 (request logic) that couples input ports 12 to input queue 36 as shown in Figure 3.

"Wherein the request logic simultaneously writes data to the FIFO storage buffer for at least two of the input ports" is anticipated by controller 34 (request logic) of Figure 3 that receives data from the input ports and writes to up to four segments of the input queue at any one time (simultaneously) as spoken of on column 5, lines 14-19, as well as column 6, lines 38-40, and column 8, lines 23-31.

Lastly, "a memory in communication with the request logic, wherein the memory concurrently maintains a plurality of pointers, wherein each pointer in the plurality of pointers corresponds to a different location in the FIFO storage buffer for storing data from an input port in the set of input ports" is anticipated by the RAM 50 (memory) of the input queue 36 (FIFO storage buffer) shown in Figure 4 that maintains a plurality of pointers WRITE_POINTER_N as spoken of on column 5, lines 31-54.

Regarding claim **52**, "a first entry that maintains a pointer corresponding to a first location in the FIFO storage buffer for storing a first set of data from an input port in the set of input ports" is anticipated by WRITE_POINTER_1 shown in Figure 4 that corresponds to the first segment 52 (location) in input queue 36 where data input from the input ports is written as spoken of on column 5, lines 39-54.

Lastly, "a second entry that maintains a pointer corresponding to a second location in the FIFO storage buffer for storing a second set of data from an input port in the set of input ports" is anticipated by WRITE_POINTER_2 of Figure 4 that corresponds to the second segment 52 (location) in input queue 36 where data input from the input ports is written.

Regarding claim **53**, "a third entry that maintains a pointer corresponding to a third location in the FIFO storage buffer for storing a third set of data from an input port in the set of input ports" is anticipated by WRITE_POINTER_3 of Figure 4 that corresponds to the third segment 52 (location) in input queue 36 where data input from the input ports is written.

Lastly, "a fourth entry that maintains a pointer corresponding to a fourth location in the FIFO storage buffer for storing a fourth set of data from an input port in the set of input ports" is anticipated by WRITE_POINTER_N of Figure 4 that corresponds to the Nth segment 52 (location) in input queue 36 where data input from the input ports is written.

Regarding claim **54**, "wherein the memory maintains a data identifier for each pointer in the plurality of pointers" is anticipated by the data segments 52 of Figure 4 that each correspond to a particular pointer.

Regarding claim **55**, "wherein each data identifier identifies a data source" is anticipated by the data segments 60 shown in Figure 5 containing frame data 62 and attributes 64 corresponding to a particular input port (data source) as spoken of on column 5, lines 30-39.

Regarding claim **56**, "wherein the memory is a content addressable memory" is anticipated by the RAM 50 of Figure 4.

Regarding claim **57**, "wherein the request logic and the storage buffer are included in a multiple port memory" is anticipated by controller 34 (request logic) and input queue 36 (storage buffer) within multiple input/single output FIFO queue 10 of Figure 3.

Regarding claim **71**, "accepting data from a first data packet, wherein the data accepted is a subset of the first data packet" is anticipated by the detection of input ports having data ready to input by port combiner 30 and the subsequent forwarding (accepting) of this data to controller 34 as spoken of on column 4, lines 53-57.

"Storing the data from the first data packet in a FIFO" is anticipated by the writing of the input data into the input queue 36 by controller 34 as spoken of on column 4, lines 57-58.

"Accepting data from a second data packet at substantially the same time as the data from the first data packet, wherein the data accepted is a subset of the second

data packet and storing the data from the second data packet in the FIFO at substantially the same time as the data from the first data packet" is anticipated by controller 34 of Figure 3 that receives data from the input ports via port combiner 30 and writes to up to four segments of the input queue at any one time (substantially the same time) as spoken of on column 5, lines 14-19, as well as column 6, lines 38-40, and column 8, lines 23-31.

Regarding claim **72**, "wherein the first data packet originates from a first source and the second data packet originated from a second source" is anticipated by input ports 12 that each forward data to port combiner 30 of Figure 3.

Regarding claim **73**, "determining that the data accepted includes a first line of the first data packet, allocating a first location in the FIFO for storing data from the first data packet, determining that the data accepted includes a first line of the second data packet, and allocating a second location in the FIFO for storing data from the second data packet" is anticipated by controller 34 that writes the received input data to segments 52 (first and second locations) of RAM 50 of input queue 36 as shown in Figure 4 as spoken of on column 5, lines 39-54.

Regarding claim **74**, "creating a first pointer to the first location and creating a first tag identifying the first data packet" is anticipated by WRITE_POINTER_1 shown in Figure 4 that corresponds to the first segment 52 (location) in input queue 36 where data input from the input ports is written as spoken of on column 5, lines 39-54.

Regarding claim **75**, "creating a second pointer to the second location and creating a second tag identifying the second data packet" is anticipated by

WRITE_POINTER_2 of Figure 4 that corresponds to the second segment 52 (location) in input queue 36 where data input from the input ports is written.

Regarding claim **76**, "wherein the first tag identifies a source of the first data packet and the second tag identifies a source of the second data packet" is anticipated by WRITE_POINTER_1 and WRITE_POINTER_2 that associate a particular data segment with a corresponding input port.

Regarding claim **77**, "accepting additional data for the first data packet, determining that the additional data accepted does not include a first line of the first data packet, identifying a position in the first location in the FIFO for storing the additional data from the first data packet, accepting additional data for the second data packet, determining that the additional data accepted does not include a first line of the second data packet, and identifying a position in the second location in the FIFO for storing the additional data from the second data packet" is anticipated by controller 34 that writes the received input data to segments 52 (first and second locations) of RAM 50 of input queue 36 as shown in Figure 4 as spoken of on column 5, lines 39-54.

Regarding claim **78**, "retrieving a pointer to the position in the first location and retrieving a pointer to the position in the second location" is anticipated by WRITE_POINTER_1 and WRITE_POINTER_2 that associate a particular data segment with a corresponding input port.

Regarding claim **79**, "accepting additional data for the first data packet, determining that the additional data accepted includes a last line of the first data packet, purging a pointer to a position in the first location in the FIFO, accepting additional data

for the second data packet, determining that the additional data accepted includes a last line of the second data packet, and purging a pointer to a position in the second location in the FIFO" is anticipated by controller 34 that writes the received input data to segments 52 (first and second locations) of RAM 50 of input queue 36 as shown in Figure 4 as spoken of on column 5, lines 39-54 as well as the incrementing (purging) of write pointers upon the completion of written segments of RAM 50 as spoken of on column 5, lines 39-54.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims **58-66** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mann et al. (U.S. 6,212,165) (hereinafter "Mann").

Regarding claims **58 and 66**, *Mann* teaches data network device 70 (switch) of Figure 2 having input ports 12 and multiple input/single output FIFO queue 10 (sink port) that receives input data from input ports 12 via port combiner 30. *Mann* also teaches controller 34 of Figure 3 within multiple input/single output FIFO queue 10 that receives data from the input ports and writes to up to four segments of the input queue 36 at any one time (simultaneously) as spoken of on column 5, lines 14-19, as well as column 6, lines 38-40, and column 8, lines 23-31. *Mann* does not teach multiple sink ports in communication with input ports 12.

However, at the time of the invention, it would have been obvious to someone of ordinary skill in the art, given the teachings of *Mann*, to utilize a plurality of multiple input/single output FIFO queues 10 in order to provide queuing for a greater number of input ports 12 and increase the availability of the system.

Regarding claim **59**, *Mann* further teaches input queue 36 (FIFO storage buffer) shown in Figure 3. *Mann* also teaches controller 34 (request logic) that couples input ports 12 to input queue 36 as shown in Figure 3. *Mann* also teaches RAM 50 (memory) of the input queue 36 (FIFO storage buffer) shown in Figure 4 that maintains a plurality of pointers WRITE_POINTER_N as spoken of on column 5, lines 31-54.

Regarding claim **60**, *Mann* further teaches WRITE_POINTER_1 and WRITE_POINTER_2 of Figure 4 that correspond to the first and second segments 52 (locations) in input queue 36 where data input from the input ports is written as spoken of on column 5, lines 39-54.

Regarding claim **61**, *Mann* further teaches WRITE_POINTER_3 and WRITE_POINTER_N of Figure 4 that correspond to the third and Nth segments 52 (locations) in input queue 36 where data input from the input ports is written as spoken of on column 5, lines 39-54.

Regarding claim **62**, *Mann* further teaches the data segments 52 (identifiers) of Figure 4 that each correspond to a particular pointer.

Regarding claim **63**, *Mann* further teaches the data segments 60 shown in Figure 5 containing frame data 62 and attributes 64 corresponding to a particular input port (data source) as spoken of on column 5, lines 30-39.

Regarding claim **64**, *Mann* further teaches the RAM 50 of Figure 4.

Regarding claim **65**, *Mann* further teaches controller 34 (request logic) and input queue 36 (storage buffer) within multiple input/single output FIFO queue 10 of Figure 3.

7. Claims **67 and 68** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mann et al. (U.S. 6,212,165) (hereinafter "Mann") in view of Dai et al. (U.S. 6,658,016) (hereinafter "Dai").

Regarding claim **67**, *Mann* does not teach a set of data rings in communication with the set of input ports and set of sink ports.

However, *Dai* teaches a packet switching fabric 10 in Figure 1 containing switching devices 12 that are coupled via a set of data rings 18 and 24.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to combine the data ring teachings of *Dai* with the

apparatus of *Mann* in order to provide a more robust system with bandwidth management as spoken of on column 4, lines 49-67 of *Dai*.

Regarding claim **68**, *Mann* does not teach where the multiple point entry FIFO includes a data input for each data ring in the set of data rings.

However, *Dai* teaches a packet switching fabric 10 in Figure 1 containing switching devices 12 that are coupled via a set of data rings 18 and 24.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to combine the data ring teachings of *Dai* with the apparatus of *Mann* in order to provide a more robust system with bandwidth management as spoken of on column 4, lines 49-67 of *Dai*.

Allowable Subject Matter

8. Claims **69 and 70** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim **69**, *Mann* as well as the other prior art of record fails to teach where the first sink port snoops data packets on each data ring in the set of data rings and determines whether to accept a first data packet based on a set of criteria, the criteria including: the first sink port having sufficient storage space for storing the first data packet, the first sink port supporting a destination targeted by the first data packet,

and a total number of packets being received by the first sink port not exceeding a predetermined number of packets.

Regarding claim **70**, *Mann* as well as the other prior art of record fails to teach where the first sink port includes: a ring interface coupled to the set of data rings to accept data from a plurality of sources and supply the data on a plurality of outputs, a multiple entry point FIFO in communication with the plurality of outputs on the ring interface to receive and store the data from the ring interface, and an output port coupled to the multiple entry point FIFO to receive data from the multiple entry point FIFO and transmit the data from the multiple entry point FIFO on a communications link.

Response to Arguments

10. Applicant's arguments with respect to claims **39-68 and 71-79** have been considered but are moot in view of the new ground(s) of rejection provided above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Moore, Jr. whose telephone number is (571) 272-3168. The examiner can normally be reached on Monday-Friday (8:00am - 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached at (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael J. Moore, Jr.
Examiner
Art Unit 2616

mjm MM

Seema S. Rao 7/8/06
SEEMA S. RAO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600